NC7SZ05 TinyLogic® UHS Inverter (Open Drain Output)

General Description

FAIRCHILD

SEMICONDUCTOR

The NC7SZ05 is a single Inverter with open drain output stage from Fairchild's Ultra High Speed Series of TinyLogic®. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a very broad V_{CC} operating range. The device is specified to operate over the 1.65V to 5.5V V_{CC} range. The input and output are high impedance when V_{CC} is 0V. Inputs tolerate voltages up to 6V independent of V_{CC} operating voltage. The operate soltages up to 6V independent of V_{CC} when in the high impedance state.

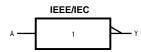
Features

- Space saving SOT23 or SC70 5-lead package
- Ultra small MicroPak[™] leadless package
- Open drain output for OR tied applications
- Ultra High Speed; t_{PD} 1.9 ns Typ into 50 pF at 5V V_{CC}
- High Output I_{OL} Drive; +24 mA at 3V V_{CC}
- Broad V_{CC} Operating Range; 1.65V to 5.5V
- \blacksquare Matches the performance of LCX when operated at 3.3V V_{CC}
- Power down high impedance inputs/output
- Overvoltage Tolerant inputs facilitate 5V to 3V translation
- Patented noise/EMI reduction circuitry implemented

Ordering Code:

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7SZ05M5X	MA05B	7Z05	5-Lead SOT23, JEDEC MO-178, 1.6mm	3k Units on Tape and Reel
NC7SZ05P5X	MAA05A	Z05	5-Lead SC70, EIAJ SC-88a, 1.25mm Wide	3k Units on Tape and Reel
NC7SZ05L6X	MAC06A	C6	6-Lead MicroPak, 1.0mm Wide	5k Units on Tape and Reel

Logic Symbol



Pin Descriptions

Pin Names	Description
A	Input
Y	Output
NC	No Connect

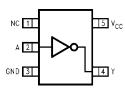
Function Table

Y =	Ā
Input	Output
Α	Y
L	*H
н	L

H = HIGH Logic Level L = LOW Logic Level *H = HIGH Impedance output state (Open Drain)

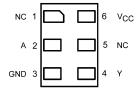
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(Top View)

Pad Assignments for MicroPak



(Top Thru View)

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Absolute Maximum Ratings(Note 1)

Supply Voltage (V _{CC})	-0.5V to +6V
DC Input Voltage (V _{IN})	-0.5V to +6V
DC Output Voltage (V _{OUT})	-0.5V to +6V
DC Input Diode Current (IIK)	
$@V_{IN} < -0.5V$	–50 mA
@ V _{IN} > 6V	+20 mA
DC Output Diode Current (I _{OK})	
@V _{OUT} < -0.5V	–50 mA
@ $V_{OUT} > 6V$, $V_{CC} = GND$	+20 mA
DC Output Current (I _{OUT})	+50 mA
DC V _{CC} /GND Current (I _{CC} /I _{GND})	±50 mA
Storage Temperature (T _{STG})	$-65^{\circ}C$ to $+150^{\circ}C$
Junction Temperature under Bias (T_J)	150°C
Junction Lead Temperature (T1);	
(Soldering, 10 seconds)	260°C
Power Dissipation (P _D) @ +85°C	
SOT23-5	200 mW
SC70-5	150 mW

Recommended Operating Conditions (Note 2)

Supply Voltage Operating (V_{CC})	1.65V to 5.5V
Supply Voltage Data Retention (V_{CC})	1.5V to 5.5V
Input Voltage (V _{IN})	0V to 5.5V
Output Voltage (V _{OUT})	0V to 5.5V
Operating Temperature (T _A)	$-40^{\circ}C$ to $+85^{\circ}C$
Input Rise and Fall Time (t_r, t_f)	
$V_{CC} = 1.8V, 2.5V \pm 0.2V$	0 ns/V to 20 ns/V
$V_{CC}=3.3V\pm0.3V$	0 ns/V to 10 ns/V
$V_{CC}=5.0V\pm0.5V$	0 ns/V to 5 ns/V
Thermal Resistance (θ_{JA})	
SOT23-5	300°C/W
SC70-5	425°C/W
Note 1: Absolute maximum ratings are DC values b	peyond which the device

Note 1 Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specification should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

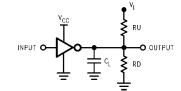
DC Electrical Characteristics

Symbol	Parameter	V _{cc}	$T_A = +25^{\circ}C$			$T_A = -40^{\circ}C$ to $+85^{\circ}C$		Unit	Conditions	
Symbol	Falanetei	(V)	Min	Тур	Max	Min	Max	Unit	Con	1110115
V _{IH}	HIGH Level Input Voltage	1.65 to 1.95	0.75 V _{CC}			0.75 V _{CC}		V		
		2.3 to 5.5	0.7 V _{CC}			0.7 V _{CC}		v		
VIL	LOW Level Input Voltage	1.65 to 1.95			0.25 V _{CC}		0.25 V _{CC}	V		
		2.3 to 5.5			0.3 V _{CC}		0.3 V _{CC}	v		
I _{LKG}	HIGH Level Output	1.65 to 5.5			±5		±10		$V_{IN} = V_{IL}$	
	Leakage Current	1.05 10 5.5			10		±ΙΟ	μΛ	$V_{OUT} = V_{CC}$	or GND
V _{OL}	LOW Level Output Voltage	1.65		0.0	0.1		0.1			
		1.8		0.0	0.1		0.1			
		2.3		0.0	0.1		0.1	V	$V_{IN} = V_{IH}$	$I_{OL} = 100 \ \mu A$
		3.0		0.0	0.1		0.1			
		4.5		0.0	0.1		0.1			
		1.65		0.08	0.24		0.24			$I_{OL} = 4 \text{ mA}$
		2.3		0.10	0.3		0.3			$I_{OL} = 8 \text{ mA}$
		3.0		0.15	0.4		0.4	V		$I_{OL} = 16 \text{ mA}$
		3.0		0.22	0.55		0.55			$I_{OL} = 24 \text{ mA}$
		4.5		0.22	0.55		0.55			I _{OL} = 32 mA
I _{IN}	Input Leakage Current	0 to 5.5			±1		±10	μΑ	$0 \le V_{IN} \le 5.5$	5V
I _{OFF}	Power Off Leakage Current	0.0			1	1	10	μΑ	V _{IN} or V _{OUT}	= 5.5V
Icc	Quiescent Supply Current	1.65 to 5.5			2.0		20	μA	V _{IN} = 5.5V, 0	GND

Symbol	Parameter	V _{cc}	T _A = +25°C			$T_A = 40^{\circ}C$ to $+85^{\circ}C$		Unite	Conditions	Figure
		(V)	Min	Тур	Max	Min	Max	Units	Conditions	Number
t _{PZL}	Propagation Delay	1.65	1.5	5.5	12.9	1.5	13.4			
		1.8	1.5	4.6	10.5	1.5	11.0	İ	$C_L = 50 \text{ pF}$	_
		2.5 ± 0.2	0.8	3.0	7.0	0.8	7.5	ns	$RU = 500\Omega$	Figures 1, 3
		3.3 ± 0.3	0.8	2.4	5.0	0.8	5.2	İ	$\text{RD}=500\Omega$	1, 0
		5.0 ± 0.5	0.5	1.9	4.3	0.5	4.5	İ	$V_I = 2 \times V_{CC}$	
t _{PLZ}	Propagation Delay	1.65	1.5	5.0	12.9	1.5	13.4			
		1.8	1.5	4.1	10.5	1.5	11.0	İ	$C_L = 50 \text{ pF}$	_
		2.5 ± 0.2	0.8	2.5	7.0	0.8	7.5	ns	$RU = 500\Omega$	Figures 1, 3
		3.3 ± 0.3	0.8	2.1	5.0	0.8	5.2	İ	$RD=500\Omega$	1,0
		5.0 ± 0.5	0.5	1.2	4.3	0.5	4.5	İ	$V_I = 2 \times V_{CC}$	
CIN	Input Capacitance	0		4				pF	İ	
C _{OUT}	Output Capacitance	0		6				pF		
C _{PD}	Power Dissipation	3.3		3.6				~ F	(Nata 2)	Figure 2
	Capacitance	5.0		6.5				pF	(Note 3)	Figure 2

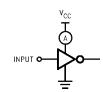
Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 2.) C_{PD} is related to I_{CCD} dynamic operating current by the expression: I_{CCD} = (C_{PD}) (V_{CC}) (f_{IN}) + (I_{CC} static)

AC Loading and Waveforms



 C_L includes load and stray capacitance Input PRR = 1.0 MHz; $t_w = 500 \text{ ns}$

FIGURE 1. AC Test Circuit



Input = AC Waveform; t_r = t_f = 1.8 ns PRR = 10 MHz; Duty Cycle = 50% **FIGURE 2. AC Test Circuit**

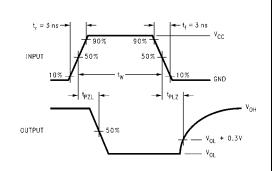


FIGURE 3. AC Waveforms

